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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARK S. CHANG, HAO FANG, and KING WAI KO

Appeal 2010-001495
Application 09/539,458
Technology Center 2800

Before HOWARD B. BLANKENSHIP, JEAN R. HOMERE, and JOHN A. JEFFERY, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-3 and 17-20. Claim 21, the only other pending claim, has been indicated as containing allowable subject matter. Ans. 5. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Appellants' invention provides contacts to a polysilicon layer in a flash memory device. *See generally* Spec. 1. Claim 1 is illustrative with a key disputed limitation emphasized:

> 1. A flash memory device comprising:
>
> a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;
>
> at least one *component* including a polysilicon layer having a top surface, wherein the at least one component is formed on a field oxide region configured to separate the plurality of gate stacks;
>
> a silicide on the top surface of the polysilicon layer of the at least one component; and
>
> an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein.

The Examiner relies on the following as evidence of unpatentability:

Ma	US 5,939,753	Aug. 17, 1999
Lee	US 6,197,639 B1	Mar. 6, 2001 (filed July 13, 1999)

THE REJECTIONS

1. The Examiner rejected claims 1, 17, and 18 under 35 U.S.C. § 102(e) as anticipated by Lee. Ans. 3-4.[1]

2. The Examiner rejected claims 2, 3, 19, and 20 under 35 U.S.C. § 103(a) as unpatentable over Lee and Ma. Ans. 5.

[1] Throughout this opinion, we refer to (1) the Appeal Brief filed April 8, 2005 (supplemented April 28, 2008); (2) the Examiner's Answer mailed October 19, 2005; and (3) the Reply Brief filed July 19, 2005.

THE ANTICIPATION REJECTION

The Examiner finds that Lee discloses every recited feature of claim 1 including flash memory device with a "component" that the Examiner maps to Lee's polysilicon layers 57 and 63. Ans. 3, 6-7. This multi-layer "component" is said to be formed on a field oxide region (field oxide layer 53) configured to separate "gate stacks" 57a, 63a in Lee's Figure 12. *Id.*

Appellants argue that Lee's polysilicon layers 57, 63 are not a "component," nor does Lee form a component on a field oxide region as claimed. App. Br. 4-5; Reply Br. 2. Appellants add that Lee fails to form a component from one of the polysilicon layers of a gate stack as recited in claim 17. App. Br. 6; Reply Br. 3. The issues before us, then, are as follows:

ISSUES

Under § 102, has the Examiner erred by finding that Lee discloses:

(1) at least one component including a polysilicon layer, where the component is formed on a field oxide region as recited in claim 1?

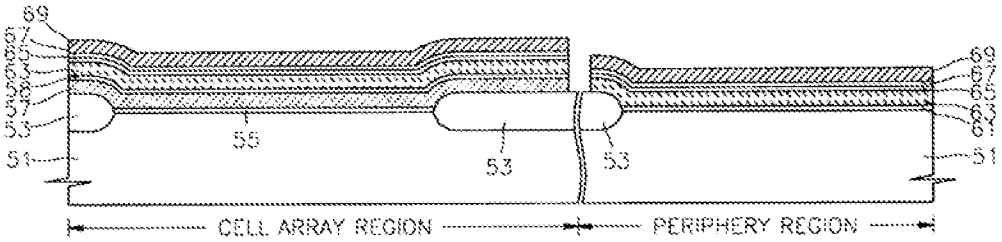
(2) the component is also formed from one of the polysilicon layers of a gate stack as recited in claim 17?

FINDINGS OF FACT (FF)

1. Appellants characterize devices utilizing a first polysilicon layer as "poly-1 components." In Figure 3B, "a poly-1 component 226 [] includes a polysilicon layer 226 and happens to be located on the field oxide region 204." Spec. 2:2-3; 6:9-10, 9:1-2; Fig. 3B.

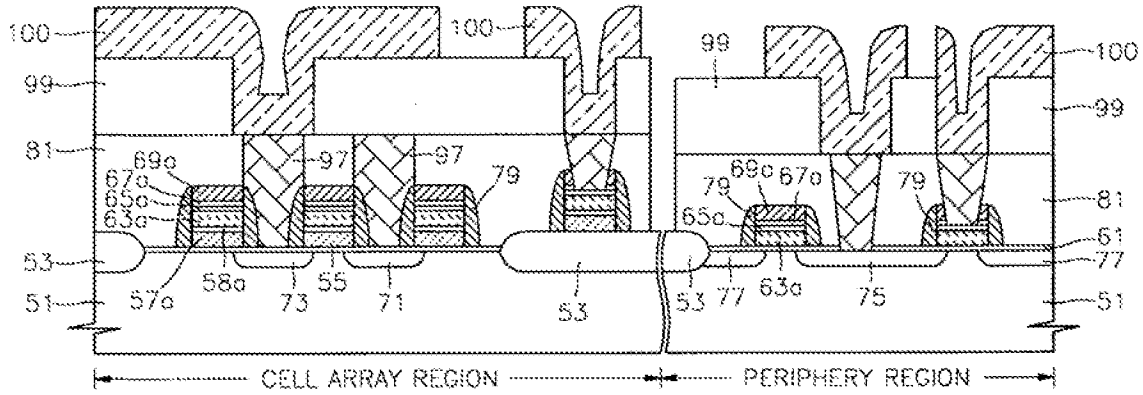
2. Lee's flash memory device is fabricated by forming field oxide layer 53 on silicon substrate 51 to define an active region. A first polysilicon layer 57 is formed on tunnel oxide layer 55 for forming a floating gate. After removing an etching mask, a second polysilicon layer 63 and tungsten silicide layer 65 are formed as a control gate in the cell array and periphery regions. Lee, col. 3, l. 35 – col. 4, l. 1; Figs. 4-6. Lee's partially-fabricated flash memory structure in Figure 6 is reproduced below:

FIG. 6



Lee's partially-fabricated flash memory structure in Figure 6

3. After further processing including patterning layers by photolithography (e.g., layer patterns 57a, 58a, 65a, 63a, 69a) to form a stack gate in the cell array region, metal layer patterns are formed to complete the flash memory device as shown in Lee's Figure 12 reproduced below. Lee, col. 4, l. 13 – col. 5, l. 64; Figs. 7-12.



Lee's completed flash memory device in Figure 12

ANALYSIS

Claim 1

This appeal turns on one key question: What is a "component"? The Examiner and Appellants disagree on this point. In particular, Appellants dispute the Examiner's equating the recited "component" to Lee's polysilicon layers 57 and 63 as noted previously. App. Br. 4-5; Reply Br. 2. We therefore begin by construing the term "component."

Appellants do not define this term, but nonetheless characterize devices using a first polysilicon layer as "poly-1 components." FF 1. Appellants label this "component" in Figure 3B with numeral 226 which, notably, matches the reference numeral for "included" polysilicon layer 226. *Id.* Based on this discussion, we therefore construe the recited "component" as a structure that includes at least one layer.

With this construction, we see no error in the Examiner's mapping Lee's polysilicon layers 57 and 63 to the recited "component" since they collectively constitute a structure including at least one layer, namely two layers. *See* FF 2-3. Nor are we persuaded of error in the Examiner's finding (Ans. 3, 6-7) that this multi-layer "component" is formed on a field oxide region, namely field oxide layer 53 both (1) before patterning in Figure 6, and (2) after patterning in Figure 12. *See id.* Although Lee uses different reference numerals for the patterned "component" layers in completed device in Figure 12 (i.e., 57a and 63a), they nonetheless correspond to the pre-patterned layers 57 and 63 that the Examiner maps to the "component" layers. *Compare* FF 2 *with* FF 3. Lee also disposes a tungsten silicide layer 65, 65a on the top surface of the "component's" polysilicon layer 63, 63a as shown in Figures 6 and 12, respectively. FF 2-3. And as the Examiner

indicates (Ans. 7), Lee covers the gate stacks, "component," and silicide with an insulating layer 81 including holes therein as claimed. FF 3.

We are therefore not persuaded that the Examiner erred in rejecting claim 1.

Claims 17 and 18

We likewise sustain the Examiner's rejection of representative claim 17 calling for the component to be also formed from one of the polysilicon layers of a gate stack. First, to the extent that Appellants argue that the recited component being formed from *one* of the gate stack's polysilicon layers precludes a multi-layer component (App. Br. 6; Reply Br. 3), we find such an argument unavailing. The scope of claim 17 does not preclude multiple polysilicon layers as the Examiner indicates (Ans. 7-8) since (1) the claim's preamble uses the open-ended term "comprising" which does not preclude additional unrecited elements,[2] and (2) the claim does not limit the recited one layer to *only one* layer. The Examiner's point in this regard (Ans. 8) is well taken.

Second, while the Examiner's identified "gate stack" in Lee may contain common elements, namely polysilicon layers 57a and 63a, Lee's gate stack is nonetheless distinct from these layers in that it also includes other patterned layers. FF 3. We therefore see no error in the Examiner's

[2] "'Comprising' is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim." *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997) (citation omitted).

position (Ans. 4, 7-8) that Lee's "component" is formed from at least one of the gate stack's polysilicon layers as claimed.

We are therefore not persuaded that the Examiner erred in rejecting representative claim 17, and claim 18 not separately argued with particularity.

THE OBVIOUSNESS REJECTION

Regarding representative claim 2, the Examiner finds that Lee's flash memory device has every recited feature except for titanium silicide, but cites Ma as teaching this feature in concluding that the claim would have been obvious. Ans. 5, 8-12.

Appellants argue that not only did the Examiner fail to evidence any motivation to modify Lee with Ma's teaching as the Examiner proposes, doing so would actually impermissibly change Lee's principle of operation. App. Br. 7-11; Reply Br. 3-4. Appellants reason that since Ma's silicide cove only covers *portions* of a polysilicon resistor, combining this teaching with Lee would allegedly render Lee unsatisfactory for its intended purpose since Lee's silicide layer 65a would no longer cover the *entire* polysilicide layer 63a. *Id.* The issues before us, then, are as follows:

ISSUES

(1) Under § 103, has the Examiner erred in rejecting claim 2 by finding that Lee and Ma collectively would have taught or suggested titanium silicide on the polysilicon layer's top surface?

(2) Is the Examiner's reason to combine the teachings of these references supported by articulated reasoning with some rational

underpinning to justify the Examiner's obviousness conclusion? This issue turns on whether combining Ma with Lee as proposed renders Lee unsatisfactory for its intended purpose.

ADDITIONAL FINDINGS OF FACT

4. Ma's titanium silicide regions 108, 109 serve as the two electrodes of polysilicon resistor 58. These electrodes are not limited to titanium silicide, but can also be formed from tungsten silicide. Ma, col. 7, l. 67 – col. 8, l. 7; Fig. 7.

PRINCIPLES OF LAW

If the Examiner's proposed modification renders the prior art unsatisfactory for its intended purpose, the Examiner has failed to make a prima facie case of obviousness. *See In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984).

ANALYSIS

Based on the record before us, we find no error in the Examiner's obviousness rejection of representative claim 2. First, we find Appellants' argument that combining Ma's teaching of using titanium silicide for Lee's silicide would allegedly render Lee unsuitable for its intended purpose unavailing. Appellants' structural argument regarding not covering the entire surface of Lee's polysilicon layer in light of Ma's portion-based coverage (App. Br. 7-11; Reply Br. 3-4) ignores the limited purpose for which the Examiner cited Ma, namely merely to show that titanium silicide is a well-known alternative to tungsten silicide—the very silicide used by

Lee. Ans. 9-11; FF 2, 4. In light of this equivalence, we see no reason why substituting tungsten silicide with titanium silicide as the Examiner proposes would not have been obvious. Doing so would not change the physical structure or orientation of Lee's silicide layer at least with respect to its coverage as Appellants seem to suggest. Rather, Lee's layer coverage would remain the same, for only the material is different under the Examiner's proposed combination. On this record, we see no reason why skilled artisans would not reasonably expect success from this substitution as the Examiner indicates (Ans. 12-13) given the express equivalence of the silicides as well as the layers' commensurate functions, namely to facilitate electrical contact with associated layers. Although Ma's semiconductor device may not be a flash memory device as Appellants argue (App. Br. 11; Reply Br. 4), its fundamental teachings are nonetheless reasonably analogous to Lee's semiconductor device at least regarding their fabrication techniques as the Examiner indicates. Ans. 9-12.

We are therefore not persuaded that the Examiner erred in rejecting representative claim 2, and claims 3, 19, and 20 not separately argued with particularity.

CONCLUSION

The Examiner did not err in rejecting (1) claims 1, 17, and 18 under § 102, and (2) claims 2, 3, 19, and 20 under § 103.

ORDER

The Examiner's decision rejecting claims 1-3 and 17-20 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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